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THE UNIVERSITY OF ALABAMA OF HUNTSVILLE

ERROR CODING SIMULATIONS

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Introduction

There are various elements such as radio frequency interference (RFI) which may induce errors in data being transmitted via a satellite communication link. When a transmission is affected by interference or other error-causing elements the transmitted data becomes indecipherable. It becomes necessary to implement techniques to recover from these disturbances. The objective of this research is to develop software which simulates error control circuits and evaluate the performance of these modules in various bit error rate environments. The results of the evaluation provides the engineer with information which helps determine the optimal error control scheme.

The Consultative Committee for Space Data Systems (CCSDS) recommends the use of Reed-Solomon (RS) and Convolutional encoders and Viterbi and RS decoders for error correction (Reference [2]). The use of forward error correction techniques greatly reduces the received signal-to noise needed for a certain desired bit error rate. The use of concatenated coding, e.g. inner convolutional code and outer RS code, provides even greater coding gain. The 16-bit Cyclic Redundancy Check (CRC) code is recommended by CCSDS for error detection (Reference [2]).

Evaluation and Implementation

The initial development phase of the simulator required evaluation of custom error correction software generated for Goddard Space Flight Center (GSFC) to determine what modules were applicable to Marshall Space Flight Center's (MSFC) planned laboratory capabilities as illustrated in Figure 1. A block diagram which illustrates the operation of the GSFC software is shown in Figure 2.

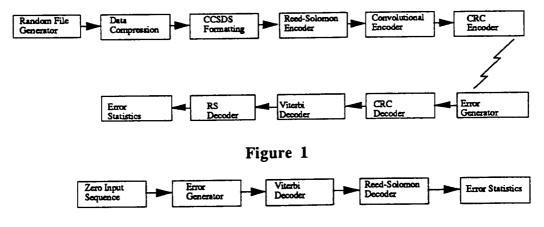


Figure 2

Since the software assumes an all zero input sequence, there is no need for an encoder because the encoded sequence will still be all zeros. This makes the task of determining the error rate a matter of only determining the percentage of non-zero decoder outputs (Reference [5]). Since MSFC's desired system requires random or user-specific data the software from Goddard is unusable in its present form. In order to provide error control capabilities for the Solar Xray Imager (SXI), the remaining modules of the CCSDS telemetry system simulator were developed. These modules include a multiplicative congruential random number generator (RNG), a random error generator, a CCSDS formatter and a CCSDS recommended CRC error detection encoder/decoder. The error statistics generator is currently being developed.

The RNG uses Equation 1 (Reference [3]):

$$X_{n+1} \equiv X_{n}p \pmod{2^k}$$
 [1]

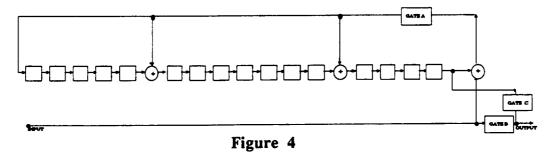
where $X_n = 1$, p = 37 and k = 15. These variables may be assigned any value but X_n and p must be odd. The RNG produces 8968 (8920 bits, maximum transfer frame length plus 48 bits, primary header length) decimal values ranging form 0 to 8191 with a period of 2^{k-2} . Binary values are generated by dividing the decimal values by 4000 and assigning 1 to resulting values greater than 0.5 and 0 to resulting values less than or equal to 0.5. The binary values are used as the random input data and the decimal values are used to access elements in the CRC-encoded message to generate errors in random order.

The CCSDS formatter inserts the sync marker $1ACFFC1D_{hex}$ (Reference [1]) at the beginning of the binary data file to conform to the CCSDS transfer frame format shown in Figure 3 (Reference [2]).

}	TRANSFER FRAME PROMARY HEADER										
ATT. AYNC MARK											
	VER	S/C ID	VIRT CHAN ID	OPER CTRL FIELD			SEC. HEADER FLAG	SYNC FLAG		SEGMENT LENGTH ID	
	2	10	3	PLAG			1	1	1	2	11
32	16			8	8	16					

Figure 3

The CRC encoder looks for the 32-bit sync marker, encodes the remaining information bits after synchronization is established and stores the first forty-eight (48) bits of the remaining bits in a header array. The error detection encoder module is the software implementation of the circuit in Figure 4 (Reference [2]).



This procedure generates a (n, n-16) code where n is the number of bits in the encoded message and n-16 is the unencoded message. Equation 2 is the 16-bit Frame Check Sequence (FCS)

$$FCS = [X^{16} \cdot M(X) + X^{(n-16)} \cdot L(X)] \text{ modulo } G(X)$$
 [2]

where M(X) is the unencoded message in the form of a polynomial, L(X) is the polynomial

used to set the 16-bit register to the all 1 state and is given by Equation 3:

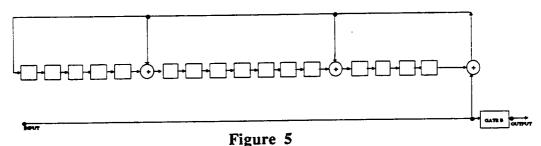
$$L(X) = \sum_{i=0}^{15} X_i$$
 [3]

and G(X) is the generating polynomial given by Equation 4:

$$G(X) = X^{16} + X^{12} + X^{5} + 1$$
 [4]

The generator polynomial has a Hamming distance of 4 therefore it is guaranteed to detect error sequences composed of one, two or three bit errors (Reference [4]). When this code is applied to a block of less than 32768 (2^{15}) bits, it also has the capability to detect all odd number of bit errors, to detect at most two bit errors, to detect all single burst errors with a length of 16 bits or less as long as there are no other errors in the block and has an undetected error probability of 2^{-15} (or 3×10^{-5}) for a random error sequence containing an even number of bit errors greater than or equal to 4.

The error detection decoder module is the software implementation of Figure 5 (Reference [2]).



Equation 5 gives the error detection syndrome.

$$S(X) = [X^{16} \cdot C^*(X) + X^n \cdot L(X)] \text{ modulo } G(X)$$
 [5]

where C*(X) is the received block in polynomial form and S(X) is the syndrome polynomial. The 16-bit register will contain all zeros if no error is detected and will contain non-zero values if an error is detected. The decoder also attempts to establish synchronization, but if a sync marker error occurs, a message will be generated to indicate this occurrence and zeros will appear in the syndrome polynomial to reflect this error.

The decoder's performance has been verified for up to 3 random errors. Tests will be performed to verify the additional performance characteristics. In generating statistics on the error detection capability, various bit error rate environments will be created and decoded for a number of successive runs. The error statistics generator will assign a one for each non-zero syndrome and a zero for each zero syndrome. It will determine the error statistics based on the percentage of non-zero terms.

Conclusion and Future Tasks

All of the previously discussed software is written in FORTRAN 77. Due to the inflexible nature of this language, e.g. input data arrays must be given a declared size, it is recommended that the code be converted to C and all future code be written in C. Appropriate error distributions must be determined so that customized error control environments may be developed. The current error correction portion of the system must be written for use with random data and user specific data. Convolutional and RS encoders and a more refined and flexible error generator must be developed. Data compression modules need to be added for the handling of "housekeeping" data. Testing of the code for various bit error rates must be continued in order to gather statistical data on the performance of the code. The process presented above provides a modular, inexpensive error control environment. Its use will allow an engineer to create an optimal error control environment for a given error distribution prior to implementing the procedure in hardware.

References

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- [4] Jain, Raj, Error Characteristics of Fiber Distributed Data Interface (FDDI), IEEE Transaction on Communications, Vol. 38, No. 8, August 1990, p. 1249.
- [5] Odenwalder, Joseph P., Error Control Coding Handbook, Final Report, Contract F44620-76-C-0056, July 15, 1976, p. 4 and p. 122.